NoteTaker System Manual

BY Douglas G. Fairbairn

April 1978

SSL-78-1xxx

ABSTRACT

This manual describes the NoteTaker computing system. NoteTaker is a portable computer of considerable power useful for a wide range of computational and simulation-oriented functions.

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road / Palo Alto / California 94304

This document is for Xerox internal use only

1.0 Introduction

The NoteTaker I is a portable computer intended for a wide variety of applications. It is a powerful personal tool intended to be its user's constant companion.

The basic components of the NoteTaker I system are as follows:

- Central CPU consisting of an Intel 8086 processor and 4K words (16 bits) of local memory.

- A minimum of 128K words (16 bits) of main memory

- A mini-floppy disk capable of storing about 340K bytes of data.

- A 7" diagonal CRT displaying 640 dots horizontally and 480 dots in the vertical direction. This provides a resolution of 118 dots/inch.

- A standard keyboard, identical to the Alto I keyboard layout.

- A pointing device, hopefuly a tablet.

- A power system capable of supplying 125 watts. The peak demand of the system is about 80 watts. There is space for batteries within the package. It is expected that the system can be operated on the batteries for about 2-3 hours at a time. A recharging system will be built into the power supply.

- An EIA interface for general purpose communications needs.

- A modem capable of operation at 300 bps. This modem has an attachment which will allow it to connect directly to a telephone through the new standard 4 pin mini-connector found on newly installed telephones.

- An analog-to-digital converter with an 8 input multiplexer on the input, and a two channel digital-to-analog converter

- An IEEE bus interface controller

- A small 2" speaker for audio output

- 8 high-voltage driver outputs

- A transparent overlay tablet for pointing on the screen

- An ethernet interface. It is not clear at this point whether the interface will reside in the package or be an external device which hangs on the bus.

- An external bus interface which allows other devices to be connected to the NoteTaker I.

- The architecture of the system is such that a small number of processors can be operated in parallel. Although these extra processors may not fit within the package, the system will offer a useful test-bed for experimenting with multi-processor architectures.

- The package is about 18" wide, 14" deep, and 6" high. The total weight without batteries is about 25 lbs.

2.0 System Architecture

A block diagram of the NoteTaker I system is shown in Fig. 1. There are three basic subsystems: the emulation processor with 4K of local memory, the I/O subsystem with its own processor and 4K of local memory, and the memory subsystem.

The emulation processor subsystem consisting of an 8086 processor with 4K of local memory. This local memory holds the machine code interpreter for the Smalltalk language. The Smalltalk byte codes and data are held in the main memory.

The memory subsystem is the second important element in the NoteTaker I. This main memory is constructed of 16K dynamic RAMs and includes single-bit error correction and double-bit detection. There are 128K words of memory using 16K chips. Memory capacity will grow to 512K when 64K memory chips become available. The memory controller consists of standard integrated circuits.

The memory is organized as 64K doublewords (32 bits). The error correction is thus done over a 32 bit word. Transfers between processors or the I/O system and memory are integer numbers of doublewords. If the requesting device requires only a word, or a byte, it must select the appropriate part of the doubleword. The memory can transfer data at the rate of about 1 doubleword every 150ns. The actual bandwidth available on the bus is thus over 200 mbs. There is no hardware limitation on how long a particular device can hold the bus, and thus no limitation on how many consecutive transfers it can take.

The third important building block of the system is the I/O section. Here we make use of as many standard LSI components as possible. The I/O system is controlled by another Intel 8086 processor. This I/O processor handles much of the overhead associated with setting up and completing I/O transfers. The communication between the I/O section and the emulation processor is handled through main memory, and a simple interrupt system.

The NoteTaker I system is designed such that one can attach multiple processors to the common memory bus. The access to the system bus is controlled with a hardware priority system involving request/acknowledge type handshaking. This multi-access capability will allow us to explore the problems and opportunities of a multiprocessor system.

3.0 Central Processor Components

The central processor of course centers around the Intel 8086 processor. This is a high performance 16-bit processor with a 20 bit address space. The processor will be provided with a local memory of 4K 16 bit words intended for storage of the 8086 code necessary for the Smalltalk interpreter. There may be some commonly used temporaries cached here as well. This memory will exist in the low-order 4K words of the 20-bit address space. Access to the main memory will be disabled if the address lies in the lowest 4K of memory. This local memory will have parity error detection.

Access to the processor and to the memory system will be gained through the Alto interface port. The Alto will be able to control the processor, load the memories, and execute other such commands therefor enabling the Alto to boot and debug the 8086 hardware and software.

4.0 Memory System

The memory system will be configured to support high-bandwidth operations. The basic memory array will be configured as 64K x 32 bits plus 7 bits for error correction and detection. These extra chips will allow the memory to correct single bit errors and

detect double bit errors. The memory is a shared resource on the central system bus. Access to the memory and thus to the bus will be granted on a fixed priority basis to one of the requestors at one time. The memory will be able to respond to 8 such requestors. When a given device wants access to the bus, it raises a memory request line. That line must be synchronized with the other requestors at the end of the current memory cycle and the one with the highest priority will gain access on the next memory cycle. The request lines will be individual while the acknowledgement will be encoded.

Once a requestor has gained access to the memory, it can control the type of transfer in the following ways:

Access Code	Action
00	Refresh
01	Read
10	Write
11	Read-Modify-Write

The data bus for the NoteTaker I will be 32 bits wide with a twelve-bit address bus. The addresses will be multiplexed into the controller. The bank select and the high-order address bits will be tansferred in the first bus cycle and the last 8 bits will be transferred in the second cycle.

Devices which don't need the whole 32-bit doubleword delivered to them, must pick the appropriate byte or word from the 32 bits.

Refreshing is done with a small state machine on the emulation processor board. This state machine has a timer which interrupts every 15 usec. When this happens, a memory request is made. When bus access is granted, the state of a 7-bit counter is strobed onto the bus and the access is specified as a refresh operation. All four banks of the memory are activated and one row in each chip is refreshed. The counter is then incremented by one. This cycle guarantees that all 128 row addresses are refreshed once every two milliseconds.

5.0 I/O System

The I/O system reflects the wide range of devices which are useful in a personal computer. Many of them are made up of a standard LSI component and a few supporting MSI chips. The floppy disk controller runs a single Shugart mini-floppy inside the cabinet and can operate up to two more floppy disks external of the NoteTaker package. Besides the very low level control functions required to suport the slow speed devices, the I/O processor must also do most of the bitblt operations.

5.1 I/O Processor: Intel 8086

5.2 Display Controller

The display controller actually interfaces to both the I/O bus and the memory bus. The I/O bus interface is used to load control information into the controller while the memory interface is necessary to support the bandwidth of the display. The packaged display requires a 12 mbs bandwidth from the memory (2.6 usec./doubleword). The controller can support displays with line rates up to 1023 lines/frame and a bandwidth of 20 mbs.

The parameters which must be loaded from the I/O processor are

1) Horizontal sync tme
2) Vertical sync time
3) Starting address of bit map
4) The number of the first visible horizontal line
5) The number of doublewords to be displayed

The sync generator furnishes an interrupt to the I/O processor every frame time. One of the operations which must be done every frame time is to change the position of the cursor on the display. There is no hardware to support this function.

The display bit map must be contiguous; the display controller cannot follow pointers in memory, etc. The bit map must also be full: there wil probably be no facility for statrting on an arbitrary scan line and finishing on another.

5.3 Slow I/O Devices

5.3.1 Keyboard

The keyboard interfaces to the keyboard controller with a serial stream of data. The power is also switched to the keyboard to minimize overall current drain. The data which comes form the keyboard is transmitted in 8 bit character format with start and stop bits, just as occurs when transmitting data over an RS232 interface. In this case however, the data comes in groups of 9 or 10 characters, where each character holds the state of 8 of the keyboard keys. The data is received and transmitted with a standard UART. This interface offers the nice capability of connecting a standard ASCII keyboard to the same line at any time and merely changing the interpretation of the data! The only difference in this case is that the normal keyboard will not send data unless requested on a separate line. The speed of the transmission will probably be about 100 usec. per character.

The layout of the keyboard will probably be a slightly modified version of the Alto I keyboard layout. The modifications might be to move the BS key in closer, make the CNTRL key single width and add a key which was "off-on" whcih did the same thing as CNTRL and CNTRL-SHIFT in present operations. In addition another key might be added to the right of the blank key on the bottom row to do . . . let's see what was it going to do?

5.3.2 Tablet

We are presently considering the use of the Thornburg tablet as a cursor control and drawing tablet. If the tablet is not suitable for this, we will at least use it as a method of pointing at the screen. The unit will mount in a bezel at the front of the CRT and will be removable.

If this tablet technology does not prove feasible as a drawing medium, we will probably stick with the mouse.

5.3.3 EIA Interface

The EIA interface for the system will be available to drive the modem or to drive an EIA RS232 line directly. There will be a standard 25 pin EIA connector (?) in the rear of the NoteTaker I so that it can be plugged into an compatible line.

5.3.5 Modem

The modem will be a custom layout of the standard Vadic 300 baud modem. This modem will have a newly-created standard 4 pin plug on it which will allow it to connect directly to newly installed phones. Phones without this jack can be used with the aid of an adapter which will allow the unit to connect directly to the mouthpiece of an ordinary telephone. (This is not strictly leagal)

5.5 Floppy Disk Controller

The floppy disk controller consists of a single chip Intel XXXX unit plus a few additional support chips. This controller runs the floppy disk which is integrated with the unit and can also control 2 external floppy disks when extra storage is required(?)

5.5 A/D and D/A

The A/D converter(~~10~~ 12-bit) will be used for general purpose analog input requirements. The D/A converters will be used for music generation and any other desired uses. The

(12)

access to these units will be through the general purpose I/O connector at the rear of the unit.

The A/D converter will have an 8 chnnel multiplexer on its front end so that it can be used for a variety of purposes. Two of the inputs will come from the tablet. Another of the inputs will be used to read the battery voltage. Other inputs might be tied to such things as pressure or temperature transducers in the outside world.

The D/A converters (10-bits) will have sample-and-hold circuitry and you will be able to run them directly into the input of your home stereo amplifier system.

5.6 High-voltage Drivers

Users of the NoteTaker will probably want to use their computer to control real-world things such as motors and light bulbs, etc. Their will thus be 8 high voltage control units which are available at the general purpose I/O connector.

5.7 Ethernet Interface

The ethernet interface will be internal to the unit if we can afford the space and power constraints.

5.8 IEEE Bus Interface

I think this is a bad idea for now. It may be added through the external I/O bus interface.

5.9 Real-Time Clock

There will be a hardware realtime clock which is run off a smallseparate battery. The clock itself should be some I^2L or CMOS clock circuit which will draw very low power and thus be allowed to operate continuously. This will preserve time over the periods the device is turned off or being carried. The clock may simply be an oscillator connected to a CMOS register which can be read from the I/O processor.

6.0 Interrupts

There is an 8 line interrupt bus which is accessable to all subsystems. The emulation processor has only one interrupt, which is the method used by the I/O processor(s) to notify it that they are done with their tasks.

The I/O processor has its own private interrupt system. One of these interrupts is from the common interrupt bus mentioned above. Another is the 60 Hz. clock which runs the vetical sync for the display. It is used to remind the I/O procesor to do some internal bookkeeping tasks such as changing the position of the cursor in the bitmap, and strobing the keyboard for data and updating the keyboard map in main memory.

7.0 System Restart (Booting)

The system can boot from either the ethernet, the modem, or the floppy disk. There is a PROM connected to the I/O procesor which allows it to determine the boot device from the keyboard and initiate the proper sequence of instructions.

When the boot button(where's that?) is depressed, all the processors execute an internal restart sequence and then try to access location 3777760B (FFFF0H). These high-order addresses will be mapped into the local address space, so each processor can have something different stored in that location.

The I/O processor will have a jump to the boot routine. The other processors will have a jump to a location in main or local memory somewhere which has a WAIT instruction stored in it. The I/O processor will do all the appropriate initialization while the other processors are waiting. When the intialization is done, the I/O procesor will set the

appropriate bit in the I/O system which is tied to the TEST pins of all the processors. When this line is asserted, all the processors in a wait state will begin processing at the location after the WAIT instruction. Note that they all could have been looking at a different WAIT statement, so they all can begin processing at different locations.

8.0 Error Conditions

When a main memory error occurs, and the memory interface has to correct a single bit error, the error must be reported so records of bad chips can be kept. The logging of errors is handled by the I/O processor.

Everytime an address is strobed onto the memory bus, it is also loaded into a register on the I/O board. When the data associated with that address is read from the memory, it also is strobed into this register, along with the error syndrome from the error checker. When an error occurs, loading of this register is disabled and an interrupt on one of the I/O board interrupt lines is enabled. The I/O processor will read the error and record it in its own memory, on the disk, or take some other appropriate action.

If a double bit error occurs, the processor which forced the error will be rebooted. This reboot operation should probably be maskable so that it can be turned off if desired. A double bit error is also recorded in the same way as noted above. Note that in the case of single bit errors, the processor which caused the error is allowed to continue.

With the above reporting mechanism, it is obvious that errors can occur without being recorded if they happen within a short time of each other. This compromise solution was arrived at in an effort to keep package count and power consumption down.

When a processor gets an error in its local memory, a bit on the system bus interface wil be reset to map the low order 4K of main memory into the local processor's address space. The processor will then be rebooted as described above. Obviously only one processor can be so mapped and there must be an indication that this has been done. There should also perhaps be a reporting mechanism so that other processors can find out that one has been rebooted.

9.0 Disc Format

In an effort to remain compatible with other mini-floppy systems, we should probably choose to format the disk in the standard IBM, soft-sectored way. We could choose to vary this for higher density if this seemed advantageous.

10.0 Outside World Connections

Access to the various I/O systems within the NoteTaker will be as follows:

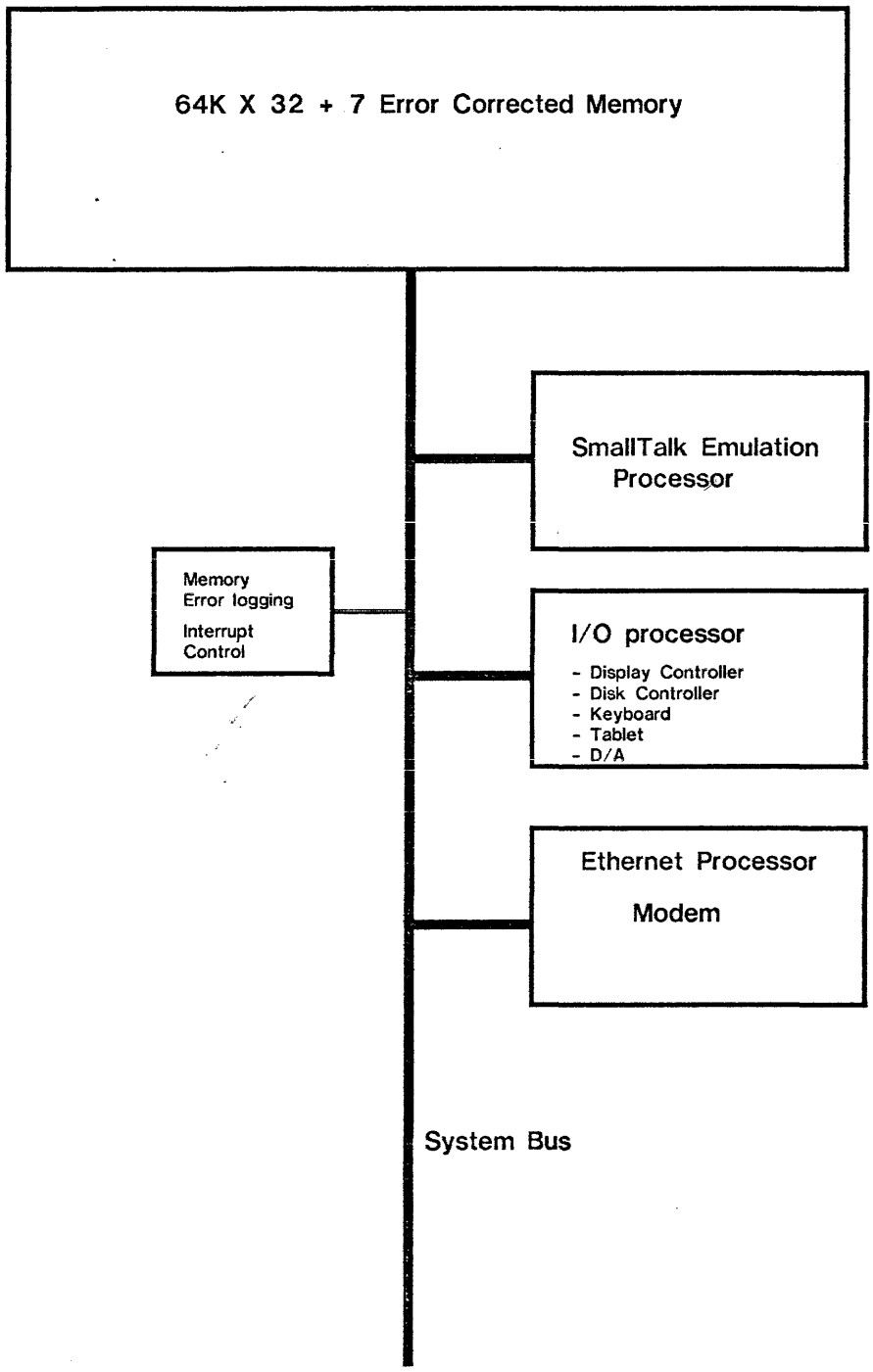
- Floppy Disks:	PCB connector on side of I/O board
- I/O processor bus:	PCB connector on side of I/O board
- Composite video:	BNC at rear of NoteTaker
- Straight video:	BNC at rear of NoteTaker
- Horiz. sync:	BNC at rear of NoteTaker
- Vertical sync:	BNC at rear of NoteTaker
- Modem:	4 pin connector at rear
- EIA:	I/O bus connector
- Ethernet:	15 pin cannon connector at rear
- System Bus:	Extender card plugged into fourth slot
- D/A:	2 RCA phono jacks at rear
- A/D:	25 pin "real world" Cannon connector
- High Voltage drivers	25 pin "real world" Cannon connector
- AC line power:	Retractable power cord

The total number of connectors involved is not as bad as it looks. The totals stand as:

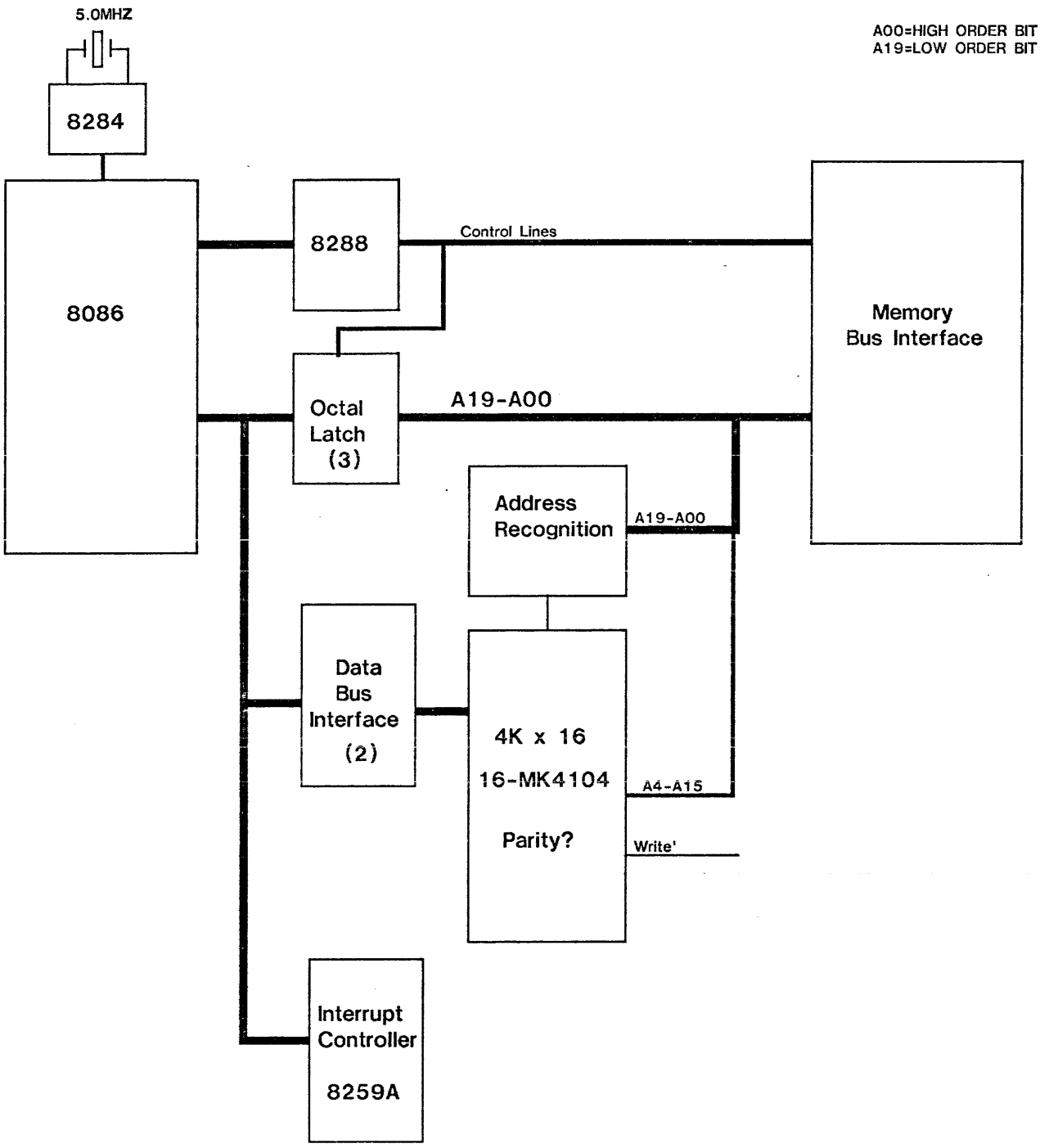
1 15 pin Cannon — ethan

1 25 pin Cannon
2 RCA phono jacks
4 BNC
1 Modem plug

In addition there must be space for cable to extender chassis, cable to the floppy disks, I/O processor bus cable, and the power cable.



NOTETAKER SYSTEM DIAGRAM



Memory Bus Interface Protocols:

1. On receipt of ALE from 8288, the MBI checks the address which is being specified and if it is not local, issues a BusReq to access the main memory.
2. The MBI returns a not READY signal to the 8086 until the BusReq is honored and the memory access is complete. It latches the data from the bus for the processor.
3. On a WRITE request, it waits to gain access to the bus as above, but releases the processor as soon as it can be guarenteed that the memory operation will be completed before the processor can make another request
4. The MBI must be prepared to accept 32 bits from the memory and provide the proper byte or word from those 32 bits as requested by the processor.
5. A more baroque implementation would call for the MBI to remember the last address it fetched data from and return the data immediately if the next reuest was for data in those original 32 bits. It is yet to be determined how much of an advantage this would be.
6. The MBI must also be capable of specifying what type of access is being made: read, write, or read-modify-write. The processor would presumably specify RMW by setting the LOCK signal on.
7. There should probably be only one interrupt line from the outside for this processor. See discusson of interrupts in the system manual.

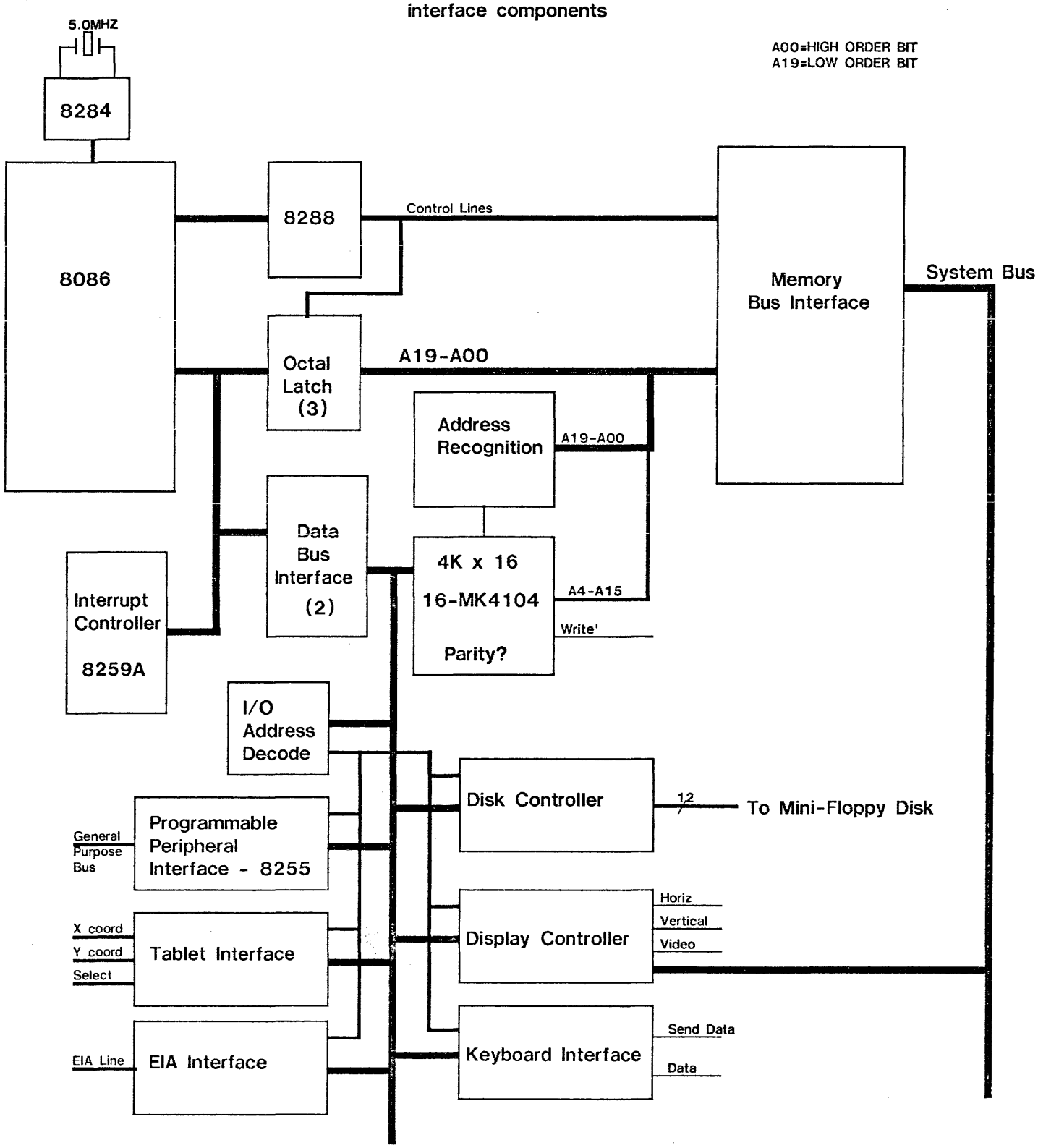
<Fairbairn>ntprocblock.sil

To be included on I/O board:

Disk Contoller	- 1LSI + 5 TTL
Display Controller	- 1 LSI 20 TTL
Keyboard interfce	- 1 LSI 2 TTL
Tablet Interface	- 2 LSI + 5 TTL (A/D)
D/A	- 1 LSI + 5 TTL
EIA-	- 1 LSI + 2TTL
	7LSI + 39 TTL +Processor and interface components

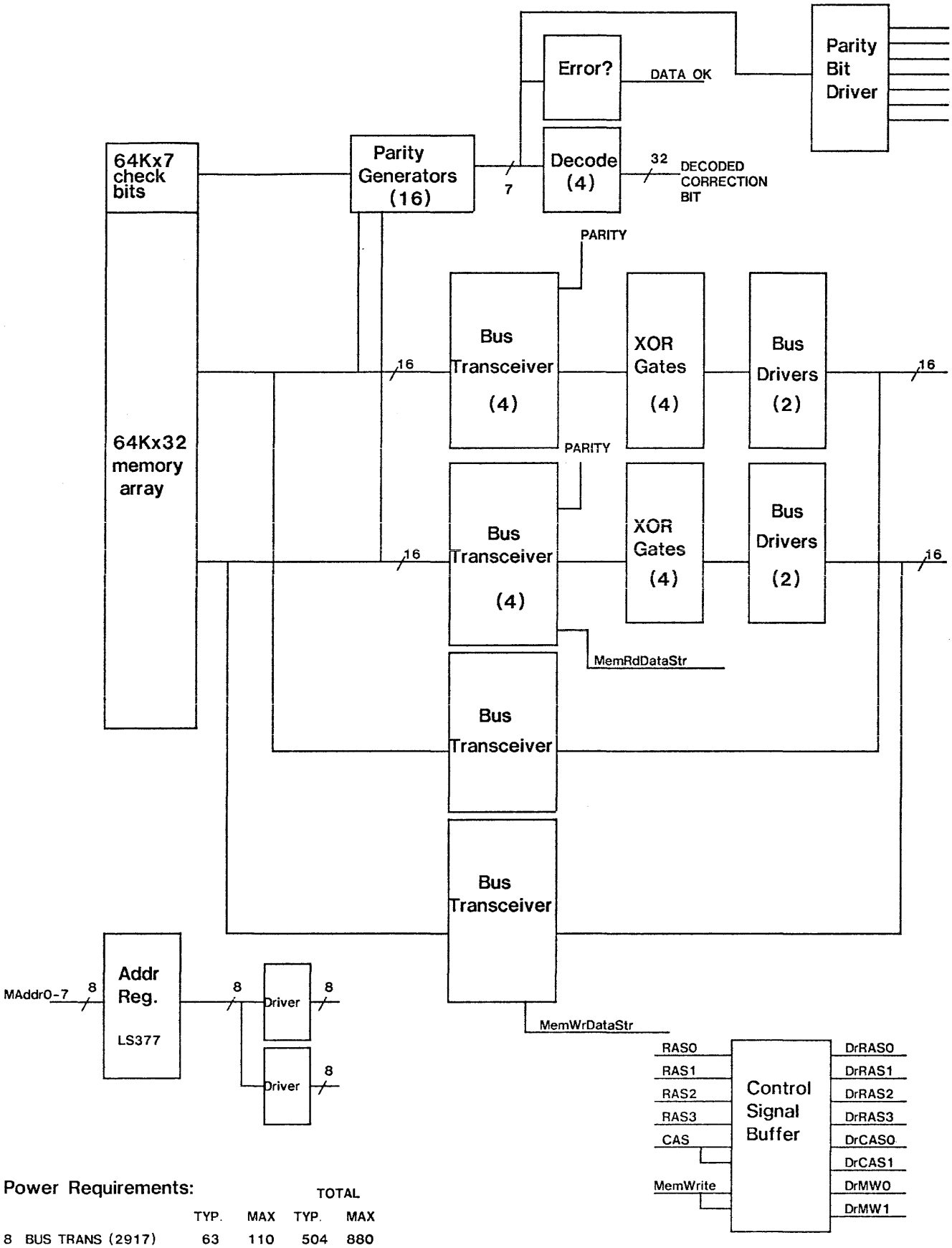
To be included on 2nd I/O board ??

High voltage interface
Ethernet
Modem
IEEE bus interface



I/O SYSTEM BLOCK DIAGRAM

<fairbairn>ntioblock.sil

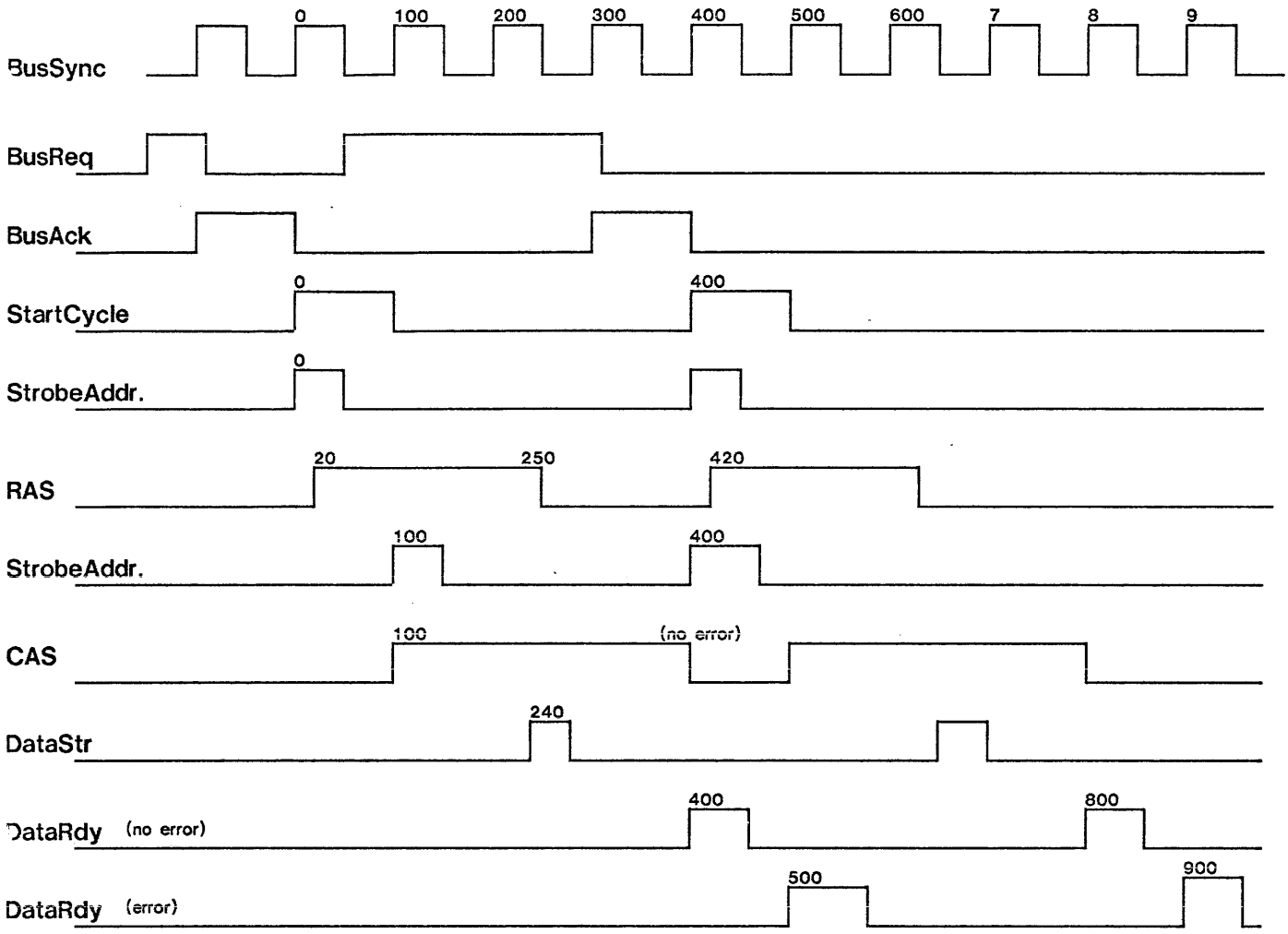


Power Requirements:

	TYP.	MAX	TOTAL TYP.	TOTAL MAX
8 BUS TRANS (2917)	63	110	504	880
8 XOR GATES (74LS86)	6	10	48	80
16 PARITY GEN. (LS280)	13.5	22	216	352
4 DECODERS (74LS138)	6	10	24	40
1 OCT. D REG. (74LS377)	17	28	17	28
8 OCT. BUS DR.(LS241)	27	46	216	368
			1025	1748 MA.

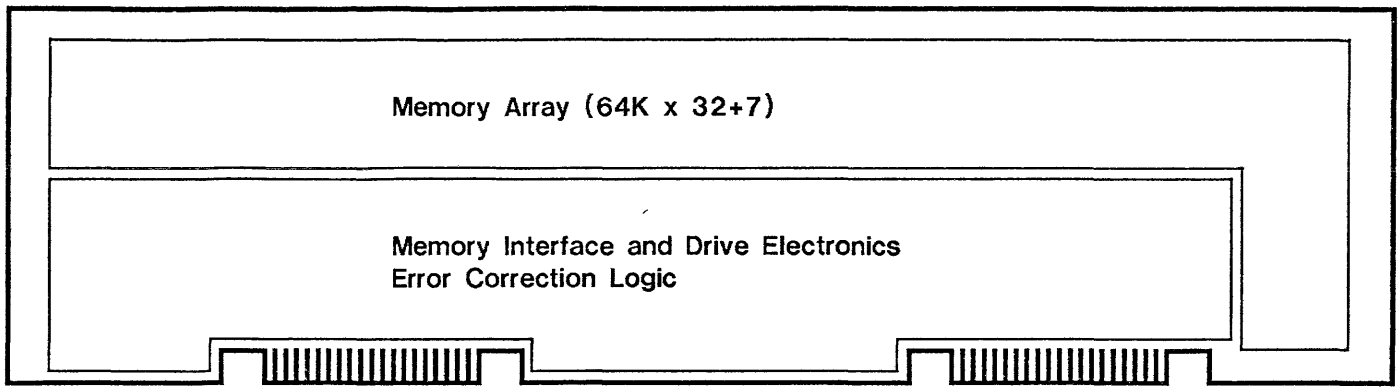
NoteTaker I Memory System

<Fairbairn>ntmemsys.sil

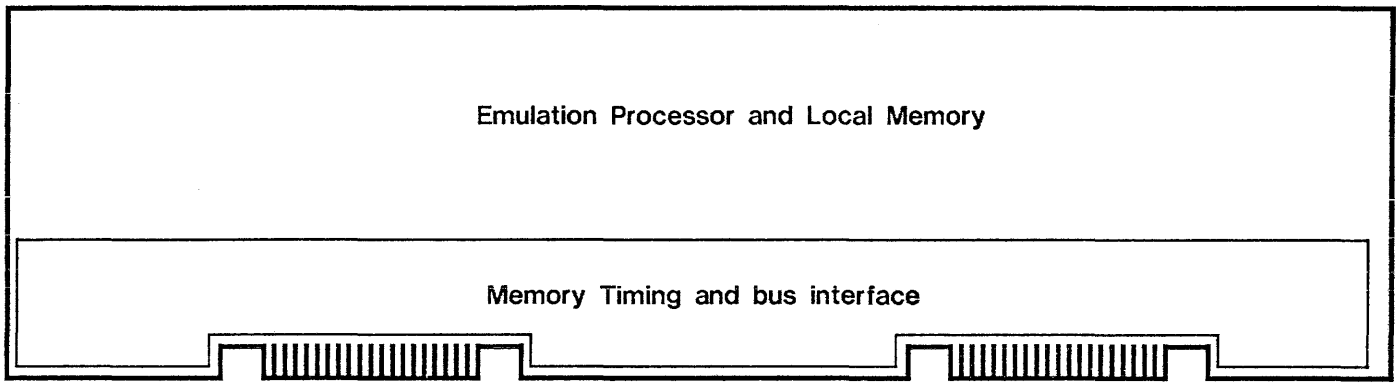


Timing Diagram for two successive READS

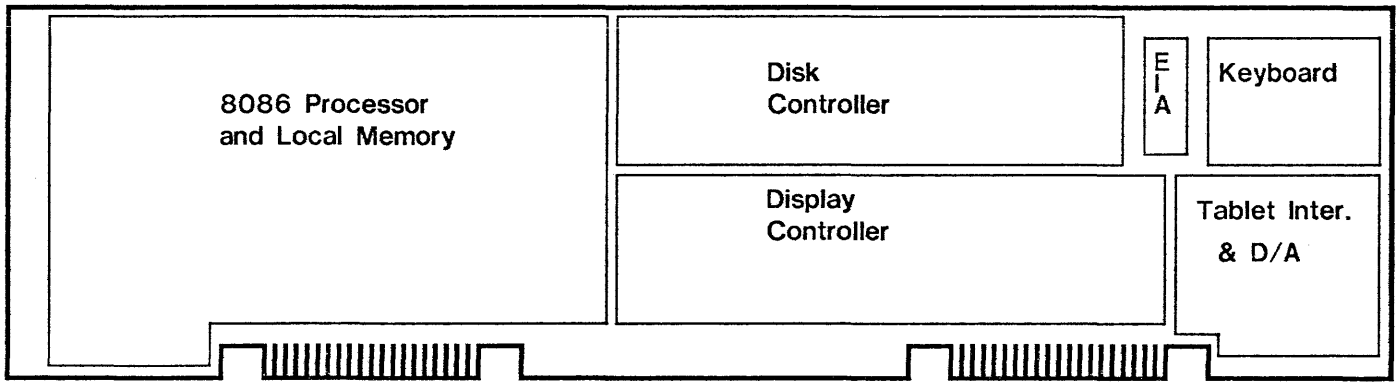
Memory Board



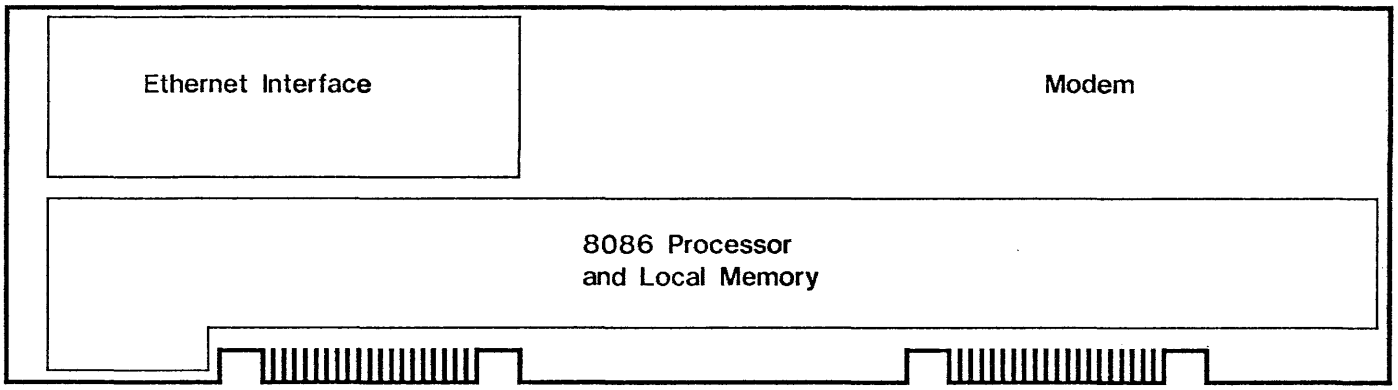
Processor Board



I/O Board



I/O Board



NoteTaker Board Layout

(DON'T TAKE IT TOO LITERALLY AT THIS POINT)

<Fairbairn>ntboards.sil